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| APPLICATION NO.  | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO.        | CONFIRMATION NO.       |
|--|-------------|----------------------|----------------------------|------------------------|
| 10/808,895   | 03/24/2004  | John R. Humphrey     | 10354*3                    | 7412                   |
| 23416 7590 06/18/2007<br>CONNOLLY BOVE LODGE & HUTZ, LLP<br>P O BOX 2207<br>WILMINGTON, DE 19899 |             |                      | EXAMINER<br>PORTKA, GARY J |                        |
|  |             |                      | ART UNIT<br>2188           | PAPER NUMBER           |
|  |             |                      | MAIL DATE<br>06/18/2007    | DELIVERY MODE<br>PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

|                              |                                      |  |  |
|------------------------------|--------------------------------------|--|--|
| <b>Office Action Summary</b> | <b>Application No.</b><br>10/808,895 | <b>Applicant(s)</b><br>HUMPHREY ET AL. |  |
|                              | <b>Examiner</b><br>Gary J. Portka    | <b>Art Unit</b><br>2188                |  |

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 26 March 2007.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-16 is/are pending in the application.  
     4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 2-16 is/are allowed.
- 6) ☒ Claim(s) 1 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
     a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                       | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

### **DETAILED ACTION**

1. Claims 1-4, 8, and 14 have been amended by Applicant. Claims 1-16 are pending.

#### ***Response to Arguments***

2. Applicant's arguments filed March 26, 2007, with regard to claim 1, have been fully considered but they are not persuasive. Applicants have argued that Placidi does not route data to each computation engine so that all data dependencies are satisfied when each read address is presented, rather, that two read operations are required. First, the cited sections of Placidi does disclose a single read cycle ("Ideally, implementing eight busses (plus 8 set of SDRAM control signals) would have allowed for fetching all of the data in a single read cycle."). Although Placidi then indicates that this adversely affects I/O pin count and signal routing, clearly this is a trade-off that would have been recognized by one of ordinary skill in the art, who would have desired the single cycle if performance rather than pin count and routing were the priority. Further, such a design decision is immaterial to the combination of Placidi with Kiamilev. The motivation for implementing dual-port memory is a separate issue that is clearly not affected by any considerations of whether Placidi "teaches against" doing this in one cycle; the design choices are still clear as stated above, with the addition of the motivation for implementing dual-port SDRAM. Second, Placidi may indeed be interpreted as satisfying the data dependencies when each read address is presented, since they are presented in parallel, the read addresses of two operations are presented

at the same time, and the data dependencies are satisfied when each of these are presented.

***Claim Rejections - 35 USC § 112***

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 1 recites "the FDTD method" at lines 1 and/or 2, which is unclear because 1) it lacks proper antecedent basis, and 2) it is not apparent if there is only one FDTD method, and if not then to which method is referred.

***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Placidi, "A Custom VLSI Architecture for the Solution of FDTD Equations", in view of Kiamilev et al., US 5,951,627.
7. As to claim 1, Placidi discloses a multiple bank memory system for acceleration of the FDTD method and routing data from them to computation engines so that all data dependencies are satisfied when each read address is presented. See Abstract, Figs. 2 and 3, and page 574 at "3. System Architecture." Placidi does not specifically disclose that the memory is dual-port on-chip memory. The advantages of dual-port memory were well known to improve overall performance by allowing two operations in parallel,

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see Kiamilev Abstract. It would have been obvious to implement the memory banks of Placidi as dual-port to achieve the desirable advantage of improved performance. Additionally, progress in the art is steadily improving the integration of more circuitry into smaller space, which improves speed as well as lowering cost. It would have been obvious to an artisan that integrating the memory of Placidi onto the processor chip would have these advantages. Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to use dual-port on-chip memory, because this was taught and known to improve operating performance and lower costs.

***Allowable Subject Matter***

8. Claims 2-16 are allowed.

***Conclusion***

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gary J. Portka whose telephone number is (571) 272-4211. The examiner can normally be reached on M-F 9:30 AM - 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung Sough can be reached on (571) 272-6799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

June 9, 2007

Gary J Portka  
Primary Examiner  
Art Unit 2188

**GARY PORTKA**  
**PRIMARY EXAMINER**

